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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,706	07/24/2006	Takefumi Nishimuta	5000-5291	9357
27123	7590	01/27/2009	EXAMINER	
MORGAN & FINNEGAN, L.L.P. 3 WORLD FINANCIAL CENTER NEW YORK, NY 10281-2101				BELOUSOV, ALEXANDER
ART UNIT		PAPER NUMBER		
2894				
			NOTIFICATION DATE	DELIVERY MODE
			01/27/2009	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTOPatentCommunications@Morganfinnegan.com  
Shopkins@Morganfinnegan.com  
jmedina@Morganfinnegan.com

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/560,706	NISHIMUTA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	ALEXANDER BELOUSOV	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 01 October 2008.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-3,5,6 and 9-19 is/are pending in the application.  
 4a) Of the above claim(s) 14-19 is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-3,5,6 and 9-13 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>07/11/2008 &amp; 10/16/2008</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
|  | 6) <input type="checkbox"/> Other: _____ .                        |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/01/2008 has been entered.

### ***Information Disclosure Statement***

2. The information disclosure statement (IDS) submitted on 07/11/2008 & 10/16/2008. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claim(s) 1-3, 5-6 & 9-13** are rejected under 35 U.S.C. 102(b) as being anticipated by (US-2003/0102497) by Fried et al (“Fried”).

**Regarding claim 1**, Fried discloses in FIG. 7a-b and related text, e.g., a MIS transistor, comprising:

a semiconductor substrate (200 in FIG. 2b; 202 & 206 are parts of it; also, see paragraph 41; it states that non-SOI device can be made and that layer 204 is **not there** as paragraph 41

makes clear; so, for the purpose of illustration, just imagine that the line dividing 202 & 204 is gone in FIG. 7b and that it is all 202) having a surface with a principal crystal plane comprising a projecting part (206 is projection) formed directly from the surface of the semiconductor substrate (as it would be in non-SOI embodiment, as disclosed in paragraph 41) and at least one of a top surface and a side wall of the projecting part has a secondary crystal plane different from the principal crystal plane (as far as “principal crystal plane” and a “secondary crystal plane” see Abstract and FIG. 7b; this is exactly what Fried discloses);

a gate insulator (208 & 210) formed on the semiconductor substrate including the projecting part in such a way that the gate insulator covers at least a portion of the semiconductor substrate, the top surface and the side wall of the projecting part (first of all, 208 & 210 directly touch all of the above, including 204 which would be 202 in non-SOI embodiment, as was made clear above, and thus meets the limitations; furthermore, this is not shown in the FIG. 7b since it is a SOI embodiment, but, the 210 or another oxide would *inherently* be under the entire gate 212, *otherwise* the gate would short to the semiconductor substrate and the device would not operate; this is an *inherent* feature; for the purposes of demonstrating a point, and not prior art, see FIG. 8 of US-5391506 by Tada; gate insulator 30 is everywhere under the gate electrode 32; again, this is an inherent feature of MIS/MOS transistors);

a gate electrode (212) formed on the gate insulator including the projecting part, said gate electrode being elongated in the direction of a gate length and in the direction of a gate width (see FIGs. 7a-b); and

a pair of diffusion regions (paragraph 57; “the S/D **regions**... comprising the fin bodies”) formed on both sides of the gate electrode in the direction of said gate length on the semiconductor substrate including the projecting part (inherent location of S/D regions).

**Regarding claim 2**, Fried discloses in FIG. 7a-b and related text, **e.g.**, a channel width of a channel of the MIS transistor formed along with the gate insulator is defined by summation of each width of channels formed along with the gate insulator including the width and height of the projecting part (see FIG. 7b; the channel is exactly in the “projecting part”; and even though this is product-by-process limitation, the “channel” was “formed along with gate insulator”, because until the gate insulator (and gate, and source, and drain) are formed, there was no channel).

**Regarding claim 3**, Fried discloses in FIG. 7a-b and related text, **e.g.**, the gate insulator continuously covers the top surface and the side wall of the projecting part (inherent): if the gate insulator **did not** continuously cover the surface of the projecting part, the gate electrode would short to the projecting part or the substrate (as was made clear above) and the device would not be operational).

**Regarding claim 5**, Fried discloses in FIG. 7a-b and related text, **e.g.**, the MIS transistor (paragraph 2) comprising:

a semiconductor substrate (200 in FIG. 2b; 202 & 206 are parts of it; also, see paragraph 41; it states that non-SOI device can be made and that layer 204 is **not there** as paragraph 41 makes clear; so, for the purpose of illustration, just imagine that the line dividing 202 & 204 is gone in FIG. 7b and that it is all 202) having a surface with a principal crystal plane comprising a projecting part (206 is projection) formed directly from the surface of the semiconductor substrate (as it would be in non-SOI embodiment, as disclosed in paragraph 41) and at least one

of a top surface and a side wall of the projecting part has a secondary crystal plane different from the principal crystal plane (as far as “principal crystal plane” and a “secondary crystal plane” see Abstract and FIG. 7b; this is exactly what Fried discloses);

a gate insulator (208 & 210) covering at least a portion of the semiconductor substrate, the top surface and the side wall of the projecting part (first of all, 208 & 210 directly touch all of the above, including 204 which would be 202 in non-SOI embodiment, as was made clear above, and thus meets the limitations; furthermore, this is not shown in the FIG. 7b since it is a SOI embodiment, but, the 210 or another oxide would *inherently* be under the entire gate 212, *otherwise* the gate would short to the semiconductor substrate and the device would not operate; this is an *inherent* feature; for the purposes of demonstrating a point, and not prior art, see FIG. 8 of US-5391506 by Tada; gate insulator 30 is everywhere under the gate electrode 32; again, this is an inherent feature of MIS/MOS transistors);

a gate electrode (212) formed on the gate insulator thereby the gate electrode is electrically insulated from the semiconductor substrate (as explained above and evidenced by Tada reference); and

a pair of diffusion regions (paragraph 57; “the S/D **regions**... comprising the fin bodies”) of the same conductivity type (inherent feature of S/D regions) formed on both sides of the gate electrode on the semiconductor substrate (inherent location of S/D regions; 206 is part of the substrate, as was made clear above).

**Regarding claim 6,** Fried discloses in FIG. 7a-b and related text, e.g., the gate insulator continuously covers the top surface and the side wall of the projecting part (*inherent*: if the gate insulator (208 & 210) did not continuously cover the semiconductor, the gate electrode would

short to the semiconductor, and the device would not be operational, as was made clear above, and evidenced by Tada reference).

**Regarding claims 9 & 10,** Fried discloses in FIG. 7a-b and related text, e.g., wherein the MIS transistor is a signal transistor (*inherent*: transistors can be “on” or “off”, hence at least two different signals).

**Regarding claims 11 & 12,** Fried discloses in FIG. 7a-b and related text, e.g., the semiconductor substrate is a silicon substrate (paragraph 44: “**any** semiconductor material”) and the hydrogen content at an interface of the silicon substrate and the gate insulator is 10.sup.11/cm.sup.2 or less in units of surface density (Fried does not disclose **any** usage of hydrogen, hence the hydrogen content is “zero”).

Regarding the process limitations recited in claims 11 & 12 (“the gate insulator *is formed by* exposing the surface of the silicon substrate to a plasma of a prescribed inert gas so as to remove hydrogen”), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a “product by process” claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a

product, whether claimed in “product by process” claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

**Regarding claim 13,** Fried discloses in FIG. 7a-b and related text, **e.g.**, the semiconductor substrate is a silicon substrate (paragraph 44: “*any* semiconductor material”), and each of the principal crystal plane and the crystal planes of the top surface and the side wall of the projecting part are any two different crystal planes from the (100) plane, the (110) plane and the (111) plane (see paragraph 40).

#### ***Response to Arguments***

1. Applicant’s arguments filed on 10/01/2008 have been fully considered but they are not persuasive.
2. **Regarding the independent claims,** the Applicant makes two key arguments on page 11, second paragraph from the bottom: (1) that the claims require a *single* gate insulator and (2) that the projecting part needs to be formed *directly from* the surface of the semiconductor substrate.

Both arguments can be responded to by pointing out that the Examiner has changed the embodiment of the Fried reference to which he refers. It is now the non-SOI version of the device, as Fried allows for in his paragraph 41, and as the rejection of the independent claims makes clear. Therefore, the argument (2) is moot. As far as argument (1), it is also moot for at least two reasons. The first reason is because the word “covering” according to Webster does not require for the gate insulator to be “directly above”. “Covering” merely means “hiding from view”. Feature 210 (or 208) clearly covers (“hides from view”) each of the claimed elements of the device to some degree, if looked at from proper point of view. The second reason is because

claims do not require a *single* gate insulator. The claims merely require "a gate insulator", without specifying its exact nature. As long as it meets the limitations imposed on it, it is "a gate insulator".

3. The rest of Applicant's Arguments are moot in light of new grounds for rejection.

***Conclusion***

1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Belousov whose telephone number is 571-270-3209.

The examiner can normally be reached on Monday - Thursday 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander Belousov/  
Examiner, Art Unit 2894  
01/13/2009

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/Bradley K Smith/  
Primary Examiner, Art Unit 2894